CSE 260M - Homework 3A

Always show all work for full credit.

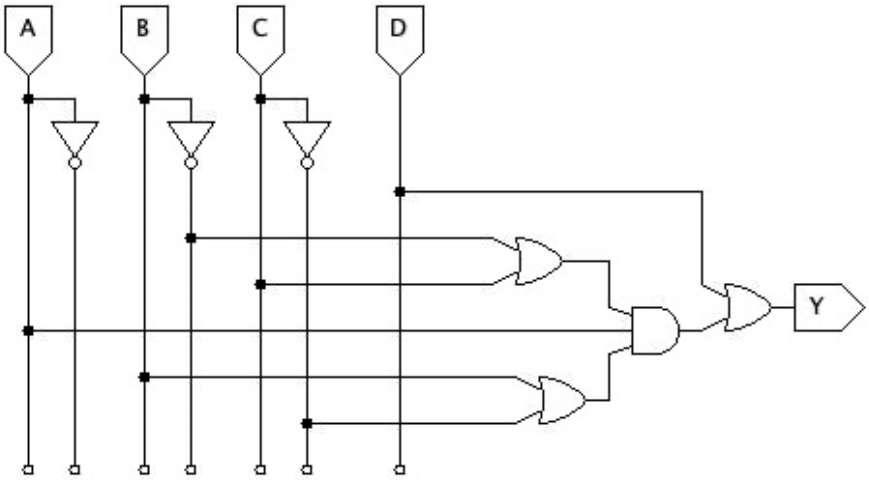
1. Determine the minimal expression (the Karnaugh map sense) for Y in:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

2. Determine the minimal expression (the Karnaugh map sense) for Y in (the Xs are “Don’t Cares”):

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	X
0	1	0	0	1
0	1	0	1	X
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

3. Given the circuit:



And the following data:

Gate	Minimum Delay (nS)	Maximum Delay (nS)
Inverter	2	5
2-input OR	8	10
2-input AND	7	11
3-input OR	9	12
3-input AND	8	11

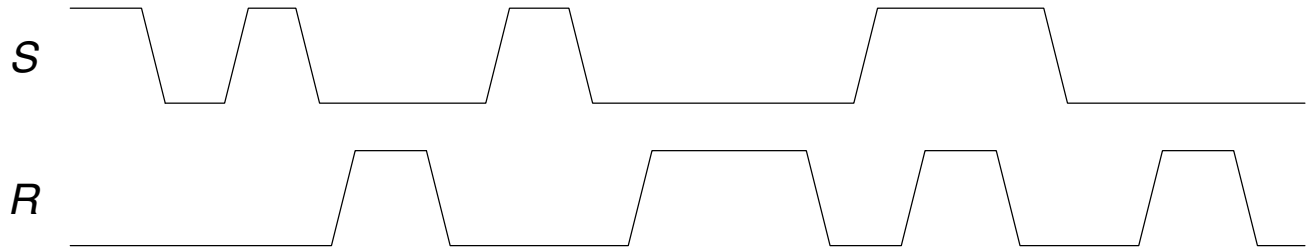
Assuming all inputs change at the same time, what is the propagation delay (t_{pd})?

4. Using the circuit and assumptions from the prior part, what is the contamination delay (t_{cd})?

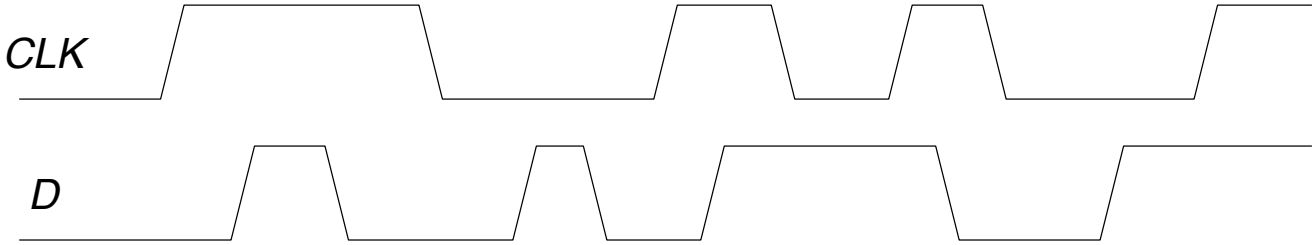
For all latch / flip-flop problems below, assume:

- Level-sensitive elements are active at high levels
- Edge sensitive elements are active on the rising edge

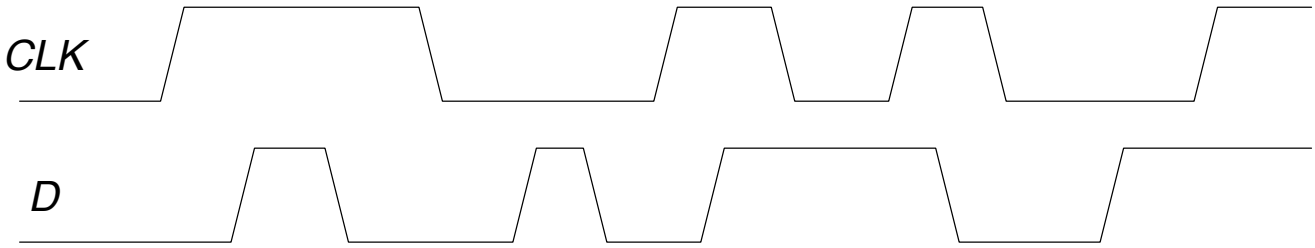
5. Given the input waveforms shown below, sketch the output, Q, of an ***SR latch***.



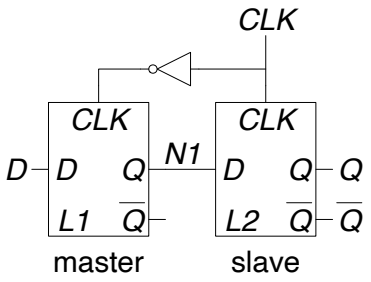
6. Given the input waveforms shown below, sketch the output, Q, of a ***D latch***.



7. Given the input waveforms shown below (same as used in the last problem), sketch the output, Q, of a ***D flip-flop***.



8. For the flip-flop shown below (Figure 3.8 of the text), *how would the behavior* change if the inverter's location were to be changed such that the clock was directly fed to the master and inverted to the slave D flip-flop? (That is, the figure below behaves as described in class/lecture. How would it behave if modified so the inverter's location was moved)



9. At a minimum, how many bits of memory are required to design a state machine that must count from 0-8?

10. At a minimum, how many bits of memory are required to design a state machine that requires n states (formula in terms of n)?

11. Assume the state machine for the traffic light state machine described in section 3.4.1 of the book uses a 5-second clock cycle, extend the state machine so that: 1) Lights are green for a minimum of 10 seconds and 2) Yellow lights continue to be 5s .(Any traffic can be ignored in the first 5s a light is green). Provide:
    1. An updated state diagram (Updated version of Figure 3.25).
       The start state should continue to be S0 (*start* (first 5s) of a green light phase in the A direction), it should continue to use the same approach to state encoding, and S0 should continue to use the code 0 (all zeros).
    2. An updated State Encoding (Table 3.2)
    3. An updated State Transition Table that includes the binary encoding (Table 3.4)
    4. An updated Output table that includes the Binary Encoding (Table 3.5)
    5. Updated equations for State variables and outputs
    6. And a JLS implementation of the machine using the provided file.