CSE 260M - Homework 2B

Always show all work for full credit.

1. Determine the minimal expression minimal (the Karnaugh map sense) for Y in:

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2. Determine the minimal expression minimal (the Karnaugh map sense) for Y in:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

3. Determine the minimal expression minimal (the Karnaugh map sense) for Y in:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

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4. Determine the minimal expression minimal (the Karnaugh map sense) for Y in:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

5. Problems 1-4 used the same functions as problems 2-5 on Homework 2. In what way are the equations optimal or minimal?

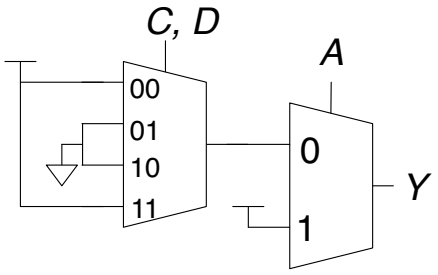
6. Determine a minimal (the Karnaugh map sense) form of:

$$Y = BC + \bar{A}\bar{B}\bar{C} + B\bar{C}$$

7. Determine a minimal (the Karnaugh map sense) form of:

$$Y = \overline{A + \bar{A}B + \bar{A}\bar{B}} + \overline{A + \bar{B}}$$

8. Give the minimized (the Karnaugh Map sense) Boolean equation for the function performed by (note that the "T" in the upper left and connecting to the bottom input of the right-most MUX represent a voltage source (that is, a logic 1) and the triangle represents a ground (that is, a logic 0):



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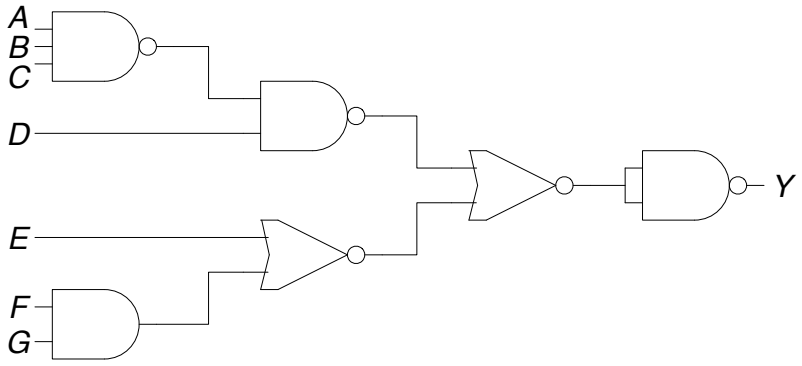
9. Use an 8-to-1 Multiplexor to implement the same function from the previous problem.

10. Assuming the propagation delays are:

Gate	t_{pd} (ps)
NOT	15
2-input NAND	20
3-input NAND	30
2-input NOR	30
3-input NOR	45
2-input AND	30
3-input AND	40
2-input OR	40
3-input OR 55	55
2-input XOR	60

Determine the propagation delay of:



11.1 Complete the full truth table for the multiplexor with enable (described on assignment page):

11.2 Find the full, canonical sum-of-products equation for it.

11.3 (JLS Submission)

11.4 What is the Propagation delay in JLS (using default delays)? (You can right-click on gates and select "Change Timing" to examine their default timing values, but do not change them).

11.5 Give the minimized (the Karnaugh Map sense) Boolean equation for the function.

11.6 (JLS Submission)

11.7 What is the Propagation delay in JLS (using default delays) of the minimized circuit?

11.8 Compare and contrast the minimal (K-Map) version with the full Sum-of-Products version.

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